AMENDMENTS TO THE SPECIFICATION

In paragraph [0026]:

As shown in Figs. 10-12, a photo resist layer (not shown) is formed on the substrate 40 after removing the reduced patterned photo resist layer 54. Then, a third photo-etching process is performed. During the third photo-etching process, a patterned photo resist layer 62 is first formed to cover the gate electrode 58 of the NLTPS TFT 70 and the channel area of the PLTPS TFT region IV, then the conductive layer 46, which is not covered by the patterned photo resist layer 62, is removed to form a gate electrode 64 of the PLTPS TFT 72. The patterned photo resist layer 62 is used to define the gate electrode 64 of the PLTPS TFT 72 and to protect the gate electrode 58 of the NLTPS TFT 70, and the patterned photo resist only needs to cover the gate electrode 64 of the ~~NLTPS TFT~~ PLTPS TFT 72. Since the gate electrode 64 is well protected, a tiny alignment error is tolerable during the photo process.